



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,215	02/25/2002	Christopher Bentley Dornan	550-316	2852
23117	7590	12/22/2004	EXAMINER	
NIXON & VANDERHYE, PC 1100 N GLEBE ROAD 8TH FLOOR ARLINGTON, VA 22201-4714				ROCHE, TRENTON J
		ART UNIT		PAPER NUMBER
				2124

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/081,215	DORNAN ET AL.
	Examiner Trent J Roche	Art Unit 2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 25 February 2002.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-39 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-39 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 25 February 2002 is/are: a) accepted or b) objected to by the Examiner.
 _____ Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>05142002, 03312004</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is responsive to communications filed 25 February 2002.
2. Claims 1-39 have been examined.

Information Disclosure Statement

3. The information disclosure statements submitted on 14 May 2002 and 31 March 2004 have been considered by the Examiner. It is noted, however, that the reference titled "A Pipeline Push-Down Stack Computer" by H. Stone is an almost unreadable document, and as such, has been considered on to the extend to which the Examiner can read the reference, mainly the title and section headings. A clean copy of the reference is required for full consideration of the text of the reference.

Claim Objections

4. Claims 1-15 are objected to because of the following informalities: "Apparatus..." should be referred to as "An apparatus..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
6. Claims 12 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Art Unit: 2124

7. Claim 12 recites the limitation "said software interpreted group" in line 1. There is insufficient antecedent basis for this limitation in the claim. As claim 2 introduced the concept of "a software interpreted group," for purposes of examination, the claim will be interpreted to read "An apparatus as claimed in claim 2..."

8. Claim 27 recites the limitation "said software interpreted group" in line 1. There is insufficient antecedent basis for this limitation in the claim. As claim 17 introduced the concept of "a software interpreted group," for purposes of examination, the claim will be interpreted to read "A method as claimed in claim 17..."

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-8, 10-23, 25-34 and 36-39 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,820,252 to Sakamoto et al, hereafter referred to as Sakamoto.

Per claim 1:

Sakamoto discloses:

Art Unit: 2124

- An apparatus for processing data under control of a set of program instructions that map upon interpretation to data processing operations to be performed (Note Figure 10 and the corresponding sections of the disclosure.)
- a fixed mapping hardware interpreter operable to interpret a fixed mapping group of said set of program instructions, whereby a program instruction from said fixed mapping group maps to a fixed sequence of one or more data processing operations (“the code read out from the program counter is directly provided to processing unit since it is native code...” in col. 10 lines 50-52. The native code is fixed to map directly to the processing unit.)
- a programmable mapping hardware interpreter operable to interpret a programmable mapping group of said program instructions, whereby a program instruction from said programmable mapping group maps to a sequence of one or more data processing operation that varies in dependence upon programming of said programmable mapping hardware interpreter (“converts the instruction, if it is non-native code, which is read out from the address...into a native code of processing unit...and provides the result to processing unit...” in col. 8 lines 52-56. The conversion programmatically maps the instructions.) substantially as claimed.

Per claim 2:

The rejection of claim 1 is incorporated, and further, Sakamoto discloses a software execution unit operable to interpret at least a software interpreted group of program instructions as claimed (Note Figure 9, item 424 and the corresponding sections of the disclosure)

Per claim 3:

The rejection of claim 2 is incorporated, and further, Sakamoto discloses one or a combination of a software interpreter and a just in time compiler as claimed (Note Figure 9, item 424 and the corresponding sections of the disclosure)

Per claim 4:

The rejection of claim 1 is incorporated, and further, Sakamoto discloses a fixed set of sequences of one or more data processing operations to which program instructions from said programmable mapping group may be mapped as claimed ("a predetermined instruction group as a native code..." in col. 3 lines 40-41)

Per claim 5:

The rejection of claim 1 is incorporated, and further, Sakamoto discloses a programmable translation table that translates program instructions within said programmable mapping group into a sequence of one or more data processing operations to be performed as claimed (Note at least Figure 21 and the corresponding sections of the disclosure.)

Per claim 6:

The rejection of claim 5 is incorporated, and further, Sakamoto discloses specifying a sequence of one or more data processing operations to be performed as claimed (Note at least Figure 21 and the corresponding sections of the disclosure.)

Per claim 7:

The rejection of claim 6 is incorporated, and further, Sakamoto discloses said programmable translation table is a content addressable memory addressed via a program instruction value to specify a corresponding operation value (Note at least Figure 21 and the corresponding sections of the disclosure. The table is addressed via the non-native code ‘`iconst_{n}`’ which is then used to translate to a specified native code.)

Per claim 8:

The rejection of claim 6 is incorporated, and further, Sakamoto discloses a random access memory with a program instruction value being decoded to address a storage location within said random access memory for a corresponding operation value as claimed (“the native code of the converted result is stored in the software cache set in RAM...” in col. 9 lines 13-14)

Per claim 10:

The rejection of claim 1 is incorporated, and further, Sakamoto discloses processing operations equivalent to one or more native program instructions of a processor core that is a target for said fixed mapping hardware interpreter and said programmable mapping hardware interpreter as claimed (Note at least Figure 21 and the corresponding sections of the disclosure. The native code is equivalent to the non-native bytecode.)

Per claim 11:

The rejection of claim 1 is incorporated, and further, Sakamoto discloses Java bytecodes as claimed (“Java bytecode...” in col. 7 line 45)

Art Unit: 2124

Per claim 12:

The rejection of claim 2 is incorporated, and further, Sakamoto discloses a software interpreted group including all those instructions not within said fixed mapping group or said programmable mapping group as claimed (“a software interpreter program operating on the processor to sequentially interpret a code which is non-native to the processor...” in col. 3 lines 48-50)

Per claim 13:

The rejection of claim 12 is incorporated, and further, Sakamoto discloses a software interpreted group including all of said program instructions, said software interpreter being invoked when neither said fixed mapping hardware interpreter or said programmable mapping hardware interpreter can interpret a program instruction as claimed (“a software interpreter program operating on the processor to sequentially interpret a code which is non-native to the processor...” in col. 3 lines 48-50. Further, “code by execution of the software interpreter every time a method constituted by non-native codes is called to operate the processor” in col. 4 lines 29-31)

Per claim 14:

The rejection of claim 1 is incorporated, and further, Sakamoto discloses said fixed mapping hardware interpreter and said programmable mapping hardware interpreter sharing at least some decoder hardware as claimed (Note Figure 1, item 105 and the corresponding sections of the disclosure.)

Per claim 15:

Art Unit: 2124

The rejection of claim 1 is incorporated, and further, Sakamoto discloses a translation pipeline stage with a program instruction buffer operable to store program instructions to be interpreted providing an input to said translation pipeline stage such that program instructions are subject to a programmable mapping within said translation pipeline stage prior to further interpretation as claimed (Note Figure 9 and the corresponding sections of the disclosure. The software cache acts as a buffer.)

Per claims 16-23 and 25-30:

Claims 16-23 and 25-30 recite method claims corresponding to the apparatus disclosed in claims 1-8 and 10-15, respectively, and are rejected for the reasons set forth in connection with claims 1-8 and 10-15, respectively.

Per claim 31:

Sakamoto discloses:

- a computer program product for controlling a data processing apparatus to provide interpretation of a set of program instructions that map upon interpretation to sequences of one or more data processing operations to be performed (Note Figures 1 and 10 and the corresponding sections of the disclosure.)
- mapping configuration logic operable to program a programmable mapping hardware interpreter to interpret a programmable mapping group of said program instructions, whereby a program instruction from said programmable mapping group maps to a sequence of one or more data processing operation that varies in dependence upon programming of said programmable mapping hardware interpreter ("converts the instruction, if it is non-

Art Unit: 2124

native code, which is read out from the address...into a native code of processing unit...and provides the result to processing unit..." in col. 8 lines 52-56. The conversion programmatically maps the instructions.) substantially as claimed.

Per claims 32-34, 36, 37, 38 and 39:

Claims 32-34, 36, 37, 38 and 39 recite computer program product claims corresponding to the apparatus disclosed in claims 4-6, 10, 11, 2 and 3, respectively, and are rejected for the reasons set forth in connection with claims 4-6, 10, 11, 2 and 3, respectively.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 9, 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,820,252 to Sakamoto et al, hereafter referred to as Sakamoto, in view of U.S. Patent 6,332,215 to Patel et al, hereafter referred to as Patel.

Per claim 9:

The rejection of claim 5 is incorporated, and further, Sakamoto does not explicitly disclose an invalid entry trap operable to block storage of unsupported mappings within said translation table.

Art Unit: 2124

Patel discloses in an analogous Java bytecode acceleration system an invalid entry trap as claimed (“the Java accelerator mode can produce exceptions at certain Java bytecodes. These bytecodes are not processed by the hardware accelerator...” in col. 3 lines 54-56. The exception is a trap, and the instructions are blocked from being processed by the translator.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the exception producing means of Patel with the hardware translation system disclosed by Sakamoto, as this would prevent unwanted errors and crashes from occurring in the system disclosed by Sakamoto by preventing improper translations.

Per claims 24 and 35:

Claims 24 and 35 are directed to a method and a computer program product, respectively, corresponding to the apparatus of claim 5, and are rejected for the reasons set forth in connection with claim 5.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trent J Roche whose telephone number is (571)272-3733. The examiner can normally be reached on Monday - Friday, 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2124

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trent J Roche
Examiner
Art Unit 2124

TJR



**TODD INGBERG
PRIMARY EXAMINER**